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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/941,180	08/27/2001	Hideyuki Harada	P/1071-1440	7067

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STEVEN I. WEISBURD
DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
1177 AVENUE OF THE AMERICAS
41ST FLOOR
NEW YORK, NY 10036-2714

EXAMINER	
MAYES, MELVIN C	
ART UNIT	PAPER NUMBER
1734	

DATE MAILED: 05/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/941,180	HARADA ET AL.	
	Examiner	Art Unit	
	Melvin Curtis Mayes	1734	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 4-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 4-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

(1)

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 15, 2004 has been entered.

Claim Rejections - 35 USC § 112

(2)

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

(3)

Claims 1 and 4-20 are rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for the sintered plate having a thickness less than the green layer having the cavity, does not reasonably provide enablement for the sintered plates having a thickness less than the green layer on which it is arranged. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to use the invention commensurate in scope with these claims.

According to the specification, the thickness of the sintered plate is equivalent to or less than the thickness of the green layer 36 in which the cavity is provided (pg. 13, lines 1-7). There is no description of the relationship of the thickness of the sintered plate to the green layer 37 on which the sintered plate is arranged.

Claim Rejections - 35 USC § 103

(4)

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

(5)

Claims 1, 4-7, 9-12, 14, 16, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Branchevsky 6,252,761 in view of Polinski, Sr. 5,708,570 or over Branchevsky in view of Polinski, Sr. and Jean et al. 6,008,535.

Branchevsky discloses a method of making a capacitor in a low-temperature co-fired ceramic (LTCC) substrate comprising: providing ceramic tape layers, 102, 104, 106, the first tape layer 102 having an electrode layer 110 and the second tape layer 104 having an opening 140 to provide a cavity for a capacitor; forming alternating layers of dielectric material and electrodes on the first tape layer in the opening of the second tape layer to form a capacitor; and firing the laminate. Branchevsky discloses that the dielectric layers may be formed using fired high-temperature ceramic tape (col. 4-5). Branchevsky do not disclose providing the laminate of tape with at least one restriction layer.

Polinski, Sr. teaches that to reduce or eliminate differential shrinkage induced distortion, cracking or bowing during co-firing of a LTCC substrate encapsulating an electronic component such as a capacitor, shrinkage control layers are provided on both sides of the substrate for restricting shrinkage during co-firing. The shrinkage control layers are comprised of alumina or titania which remains solid during co-firing and are removed after co-firing. Polinski, Sr. teaches that to compensate for the restricted shrinkage along the x and y directions, the substrate will shrink along the z direction (col. 2, line 38 – col. 5, line 42).

Jean et al. teach that when packaging a diode die 1 in a LTCC package formed from green tape 2, the diode die is placed into a through hole of the green tape such that the thickness of the green tape is slightly greater than that of the diode die (col. 3, lines 28-30).

It would have been obvious to one of ordinary skill in the art to have modified the method of Branchevsky for making a capacitor in a low-temperature co-fired ceramic (LTCC) substrate by providing removable non-sintering shrinkage control layers on both sides of the ceramic tape laminate, as taught by Polinski, Sr., to restrict shrinkage during cofiring of a LTCC substrate encapsulating an electronic component such as a capacitor.

By providing each of the layers of dielectric material forming the capacitor in the opening of the tape layer as fired high-temperature ceramic tape, as disclosed by Branchevsky, a sintered plate of fired first ceramic functional material having a thickness less than the thickness of the tape layer having the opening, as well less than the thickness of the tape on which it is arranged, is obviously provided in the opening in the tape layer, as claimed.

Further, it would have been obvious to one of ordinary skill in the art to have provided the laminate of layers of fired dielectric tape and electrodes of thickness less than the thickness

of the tape layer having the opening, as Polinski, Sr. teach that LTCC substrate restricted in shrinkage along the x and y directions shrinks along the z direction and Jean et al. teach that when packaging a die in an opening in a LTCC green tape for firing, the thickness of the green tape is slightly greater than that of the diode die. It would have been obvious to one of ordinary skill in the art, that since the tape layers of the LTCC substrate shrink in the z direction during co-firing while the fired dielectric tapes do not, to provide the fired dielectric tape capacitor in the opening in the green tape layer of less thickness than the tape layer such that the LTCC tape and the capacitor have the same thickness after co-firing.

(6)

Claims 8, 13, 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over the references as applied to Claim 1, further in view of Nomura et al. 5,335,139.

Nomura et al. teach that in making a multilayer ceramic chip capacitor, each dielectric layer preferable has a thickness up to about 50 μm, especially up to about 20 μm and lower thickness limit of about 0.5 μm, preferably about 2μm, and the number of dielectric layers stacked is generally from 2 to about 300, preferably from 2 to about 200 (col. 6, lines 26-34).

It would have been obvious to one of ordinary skill in the art to have modified the method of the references as combined by providing the fired dielectric tapes of the capacitor of a thickness of 100 μm or less, as Nomura et al. teach that in making a ceramic chip capacitor, the number of stacked dielectric layers is preferably from 2 to 200 and the thickness of the dielectric layers is preferably about 2 μm up to about 20 μm. By making the capacitor by laminating fired dielectric tapes of number and thickness within the preferred ranges as suggested by Nomura et

al., a capacitor of thickness which encompasses the thickness range of 100 μm or less, as claimed, is provided.

(7)

Claims 1, 4-7, 9-12, 14, 16 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kodama et al. 5,277,723 in view of Jean et al.

Kodama et al. disclose a method of producing a multilayer ceramic body comprising: making multilayer ceramic capacitors by layering and firing electrode printed and via-wired green sheets of barium titanate; printing green sheets of borosilicate glass and alumina filler with via wirings and surface wirings; in a part of the green sheets, punching holes larger than the capacitors; arranging the fired capacitors and a plurality of green sheets cut to an area larger than the capacitors so that the capacitors are positioned in the final laminate and the green sheet with holes larger than the capacitors is simultaneously provided as the layer to which the capacitors were laminated, the green sheets and capacitor positioned so that the electrodes and via-wiring of the capacitor are connected to the wirings of the green sheets; sandwiching the laminate between dimensionally stable, constraining-force-applying alumina porous plates; firing at 900°C; and removing the porous plates. The green sheets comprise 75 vol% borosilicate glass powder. Kodama et al. further disclose that the fired built-in structure can be a functional parts such as a capacitor or contain many small parts such as chip capacitors, resistors and coils (col. 7, lines 26-58, col. 13, lines 50-68, col. 27, line 28 – col. 28, line 51). Kodama et al. disclose that the laminate shrinks in the z direction but do not disclose that the fired capacitors have a thickness less than that of the green sheet having the holes.

Jean et al. teach that when packaging a diode die 1 in a LTCC package formed from green tape 2, the diode die is placed into a through hole of the green tape such that the thickness of the green tape is slightly greater than that of the diode die (col. 3, lines 28-30).

It would have been obvious to one of ordinary skill in the art to have modified the method of Kodama et al. by providing the fired capacitors of thickness less than the thickness of green sheet having the holes, as Jean et al. teach that when packaging a die in an opening in a LTCC green tape for firing, the thickness of the green tape is slightly greater than that of the diode die. It would have been obvious to one of ordinary skill in the art, that since the green sheets of the laminate shrink in the z direction during co-firing while the fired capacitors do not, to provide the fired capacitors in the holes in the green sheet of less thickness than the green sheet such that the green sheet and the capacitor have the same thickness after co-firing.

(8)

Claims 8, 13, 15 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kodama et al. in view of Nomura et al. 5,335,139.

Kodama et al. disclose that the green sheets comprise 75 vol% borosilicate glass powder and 25 vol% alumina powder filler. Kodama et al. does not disclose that the multilayer ceramic capacitor has a thickness of 100 μm or less.

Nomura et al. teach that in making a multilayer ceramic chip capacitor, each dielectric layer preferable has a thickness up to about 50 μm, especially up to about 20 μm and lower thickness limit of about 0.5 μm, preferably about 2μm, and the number of dielectric layers stacked is generally from 2 to about 300, preferably from 2 to about 200 (col. 6, lines 26-34).

It would have been obvious to one of ordinary skill in the art to have provided the multilayer ceramic capacitor in the multilayer ceramic body of Kodama et al. of a thickness of 100 μm or less, as Nomura et al. teach that in making a ceramic chip capacitor, the number of stacked dielectric layers is preferably from 2 to 200 and the thickness of the dielectric layers is preferably about 2 μm up to about 20 μm. By making the capacitor by laminating green sheets (dielectric layers) of number and thickness within the preferred ranges as suggested by Nomura et al., a capacitor (sintered plate) of thickness which encompasses the thickness range of 100 μm or less, as claimed, is provided.

Conclusion

(9)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Melvin Curtis Mayes whose telephone number is 571-272-1234. The examiner can normally be reached on Mon-Fri 7:30 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Crispino can be reached on 571-272-1226. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Melvin Curtis Mayes
Primary Examiner
Art Unit 1734

MCM
May 19, 2004